

## WHAT IS CLAIMED IS:

- 1           1.     A circuit, comprising:  
2                 a volatile memory array;  
3                 a logic circuit operable to detect a memory array tamper situation and generate at  
4     least one control signal responsive thereto; and  
5                 circuitry associated with each of a plurality of individual cells within the volatile  
6     memory array which responds to the at least one control signal and by destroying any data stored  
7     by the associated memory cell.
- 1           2.     The circuit of claim 1 wherein the circuit comprises a smart card.
- 1           3.     The circuit of claim 1 wherein the individual cells comprise 6T type cells.
- 1           4.     The circuit of claim 1 wherein each individual cell comprises a data latch, and the  
2     circuitry destroys the data stored by the data latch in response to the at least one control signal.
- 1           5.     The circuit of claim 1 wherein the data latch includes a latch node and the  
2     circuitry drives the latch node to a reference voltage.
- 1           6.     The circuit of claim 1 wherein each individual cell is connected to a bit line and  
2     the circuitry drives the bit line to a reference voltage.

1           7.     The circuit of claim 1 wherein each individual cell comprises a data latch, and the  
2     circuitry unbalances the latch in response to the at least one control signal to destroy the data  
3     stored therein.

1           8.     The circuit of claim 1 wherein each individual cell comprises a data latch having a  
2     first and a second side, and the circuitry exercises unique reference voltage control over each  
3     side of the latch in response to the at least one control signal to destroy the data stored therein..

1           9.     A memory circuit, comprising:  
2                 a data latch having a true node and a complement node; and  
3                 circuitry responsive to a control signal to short the true node to the complement  
4 node for the purpose of destroying data stored by the latch.

1           10.    The circuit of claim 9 wherein the circuitry comprises a p-channel transistor  
2 having its conduction terminals connected between the true node and the complement node and  
3 its gate connected to receive the control signal.

1           11.    The circuit of claim 9 wherein the circuitry comprises an n-channel transistor  
2 having its conduction terminals connected between the true node and the complement node and  
3 its gate connected to receive the control signal.

1           12.    The circuit of claim 9 wherein the memory circuit further includes:  
2                 a first pass gate coupling the true node to a bit line;  
3                 a second pass gate coupling the complement node to a complement bit line.

1           13.    The circuit of claim 12 wherein the data latch is coupled to a reference voltage  
2 line, further comprising a circuit which disconnects the reference voltage line from the latch  
3 when the control signal is activated.

1           14.    A memory circuit, comprising:  
2                   a data latch having a true node and a complement node;  
3                   a first pass gate coupling the true node to a bit line;  
4                   a second pass gate coupling the complement node to a complement bit line; and  
5                   a logic circuit generating a logic control signal to simultaneously activate the first  
6 and second pass gates to short the true and complement nodes to the bit line and complement bit  
7 line, respectively, for the purpose of destroying data stored by the latch.

1           15.    The circuit of claim 14 wherein the data latch is coupled to a reference voltage  
2 line, further comprising a circuit which grounds the reference voltage line when the logic circuit  
3 generates the logic control signal.

1           16.    A memory circuit, comprising:  
2                   a data latch having a true node and a complement node;  
3                   circuitry responsive to a control signal to short one of the true/complement nodes  
4 of the latch to a reference voltage for the purpose of destroying data stored by the latch.

1           17.    The circuit of claim 16 wherein the circuitry comprises an n-channel transistor  
2 having its conduction terminals connected between the one of the true/complement nodes and the  
3 reference voltage.

1           18.    The circuit of claim 16 wherein the circuitry comprises a p-channel transistor  
2 having its conduction terminals connected between the one of the true/complement nodes and the  
3 reference voltage.

1           19.    The circuit of claim 16 wherein the data latch is coupled to a reference voltage  
2 line, further comprising a circuit which disconnects the reference voltage line from the latch  
3 when the control signal is activated.

1           20.    The circuit of claim 16 wherein the memory circuit further includes:  
2                   a first pass gate coupling the true node to a bit line;  
3                   a second pass gate coupling the complement node to a complement bit line.

1           21.    A memory circuit, comprising:  
2                   a data latch having a true node and a complement node; and  
3                   circuitry responsive to at least one control signal to short both the true and  
4 complement nodes of the latch to at least one reference voltage for the purpose of destroying data  
5 stored by the latch.

1           22.    The circuit of claim 21 wherein the circuitry comprises:  
2                   a first n-channel transistor having its conduction terminals connected between the  
3 true node and the reference voltage; and  
4                   a second n-channel transistor having its conduction terminals connected between  
5 the complement node and the reference voltage.

1           23.    The circuit of claim 22 wherein the a gate of the first transistor and a gate of the  
2 second transistor receive the same control signal.

1           24.    The circuit of claim 22 wherein the a gate of the first transistor and a gate of the  
2 second transistor receive the different control signals.

1           25.    The circuit of claim 21 wherein the circuitry comprises:  
2                   a first p-channel transistor having its conduction terminals connected between the  
3 true node and the reference voltage; and

4                   a second p-channel transistor having its conduction terminals connected between  
5   the complement node and the reference voltage.

1           26.    The circuit of claim 25 wherein the a gate of the first transistor and a gate of the  
2   second transistor receive the same control signal.

1           27.    The circuit of claim 25 wherein the a gate of the first transistor and a gate of the  
2   second transistor receive the different control signals.

1           28.    The circuit of claim 21 wherein the circuitry comprises:  
2                   an n-channel transistor having its conduction terminals connected between one of  
3   the true/complement nodes and a first reference voltage; and  
4                   a p-channel transistor having its conduction terminals connected between the  
5   other of the true/complement nodes and a second reference voltage.

1           29.    The circuit of claim 21 wherein the data latch is coupled to a reference voltage  
2   line, further comprising a circuit which disconnects the reference voltage line from the latch  
3   when the control signal is activated.

1           30.    The circuit of claim 21 wherein the memory circuit further includes:  
2                   a first pass gate coupling the true node to a bit line;  
3                   a second pass gate coupling the complement node to a complement bit line.

1           31.    A memory circuit, comprising:

2                   a data latch comprising a first side associated with a true node and having a first  
3   positive reference voltage input and a second side associated with a complement node and  
4   having a second positive reference voltage input; and

5                   circuitry responsive to at least one control signal to selectively couple the first and  
6   second positive reference voltage inputs for the first and second sides of the latch, respectively,  
7   to a positive/ground voltage supply for the purpose of destroying data stored by the latch.

1           32.    The circuit of claim 31 wherein the circuitry comprises first and second NOT  
2   logic gates coupled to receive the at least one control signal and selectively connect the first and  
3   second positive reference voltage inputs for the first and second sides of the latch, respectively,  
4   to a positive/ground voltage supply in response thereto.

1           33.    The circuit of claim 31 wherein the cross-coupled data latch comprises a first p-  
2   channel transistor for the first side and a second p-channel transistor for the second side, a source  
3   terminal of the first p-channel transistor comprising the first positive reference voltage input and  
4   a source terminal of the second p-channel transistor comprising the second positive reference  
5   voltage input.

1           34.    The circuit of claim 31 wherein the memory circuit further includes:

2                   a first pass gate coupling the true node to a bit line;

3                   a second pass gate coupling the complement node to a complement bit line.



1           35.    A memory circuit, comprising:  
2                   a memory cell including a data node;  
3                   a pass gate coupling the data node of the memory cell to a bit line; and  
4                   circuitry responsive to at least one control signal to short the bit line to a reference  
5 voltage while the pass gate is activated for the purpose of destroying data stored by the memory  
6 cell.

1           36.    The circuit of claim 35 wherein the circuitry comprises a transistor having  
2 conduction terminals connecting the bit line to a reference voltage and a gate coupled to receive  
3 the at least one control signal.

1           37.    The circuit of claim 35 wherein the circuitry comprises a first transistor having its  
2 conduction terminals connecting the bit line to a first reference voltage and a second transistor  
3 having its conduction terminals connecting the bit line to a second reference voltage, the first and  
4 second transistors each having a gate coupled to receive the at least one control signal.

1           38.    The circuit of claim 35 further including a coupling circuit for selectively shorting  
2 the bit line to a word line to share charge therebetween.

1           39.    The circuit of claim 38 further including a pull up device to pull the word line up  
2 to a positive reference voltage after charge has been shared between the bit line and word line.